Amendments to the claims:

This listing of claims will replace all prior versions and listing of claims in the application.

1. (Cancelled)

2. (Previously amended) An apparatus as recited in claim 26 wherein said code generator comprises a counter.

3. (Previously amended) An apparatus as recited in claim 26 wherein said code generator comprises a random number generator.

4. (Previously amended) An apparatus as recited in claim 26 wherein said memory element comprises a multiple port memory element.

5. (Previously amended) An apparatus as recited in claim 26 wherein when in a test enabled condition said decoder maps a specific state for_each test code to a unique state of the enable signals.

6. (Previously Amended) An apparatus as recited in claim 26 wherein when in a test enabled condition said decoder maps more than one test code state to a single state of the enable signals.

7. (Cancelled)

8. (Previously Amended) A method as recited in claim 31 wherein said step of generating a test code comprises the step of generating a random number as said test code.

9. (Previously Amended) A method as recited in claim 31 wherein said step of generating a test code comprises the step of generating sequential numbers as said test code.

10. (Previously Amended) A method as recited in claim 31 and further comprising the step of driving all test enable signals to a constant value when in a test code disabled condition.

11. (Previously Amended) A method as recited in claim 31 wherein the step of mapping further comprises mapping a value for each test code to a unique state of the test enable signals.

12. (Previously Amended) A method as recited in claim 31 wherein the step of mapping further comprising mapping more than one test code to a single state of the enable signals.

Claims 13-19 (Cancelled)

Claims 20-25 (Cancelled)

26. (Previously presented) An apparatus for built in self test of a memory element in an integrated circuit, the memory element having at least one deterministic operation and at least one non-deterministic operation controllable by at least two control lines, the apparatus comprising:

a code generator accepting a seed input and generating a sequence of test codes in response to a clock signal,

a decoder accepting the test codes and remapping each test code to at least two test enable signals wherein the test enable signals logically combine with the control lines to stimulate only deterministic operations when in a test enabled condition.

27. (Previously presented) An apparatus as recited in claim 26 wherein there are at least two different memory elements and each memory element has associated with it a respective code generator and respective decoder.

28. (Previously presented) An apparatus as recited in claim 4 wherein one of the non-deterministic operations is a multiple write operation.

29. (Previously presented) An apparatus as recited in claim 4 wherein one of the non-deterministic

operations is a simultaneous read and write operation.

30. (Previously presented) An apparatus as recited in claim 26 wherein the decoder is a look up table implemented in a read only memory.

31. (Currently Amended) A method for built in self test of an integrated circuit having a memory element, the memory element having at least one deterministic operation and at least one non-deterministic operation controllable by at least two control lines, the method comprising the steps of:

generating a sequence of test codes from a seed input in response to a clock signal,

remapping the test codes to at least two test enable signals, and

logically combining the test enable signals with the control lines to ~~repeatably~~ stimulate only the deterministic operations when in a test enabled condition.

32. (Previously presented) A method as recited in claim 31 and further comprising the steps of accessing contents of the memory element to obtain a test signature of the memory element, and comparing the test signature against a reference test signature.